Programmable Array Logic Series 24

General Description

The PAL® Series 24 family compliments the PAL Series 20 family by providing two additional inputs and two additional outputs, allowing more complex functions in a single package. This new family is made feasible by the new 300 Mil-wide, 24-pin package.

In addition to providing more logic functions per chip, 24 pins allow for many natural functions which were previously unavailable in 20-pin packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-Line-to-1-Line Multiplexers
- Dual 8-Line-to-1-Line Multiplexers
- Quad 4-Line-to-1-Line Multiplexers

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production. This often simplifies not only the PC board layout, but also the board itself.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality cards and socket adapters. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 5 to 1, typically.
- Expedites and simplifies prototyping and board layout.
- Saves space with 300 Mil-wide, 24-pin DIP packages.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Last fuse reduces possibility of copying by competitors.

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Table 2-5. Part Types

Part Number	Description
DMPAL12L10	DECA 12 Input AND-OR-INVERT Gate Array
DMPAL14L8	OCTAL 14 Input AND-OR-INVERT Gate Array
DMPAL16L6	HEX 16 Input AND-OR-INVERT Gate Array
DMPAL18L4	QUAD 18 input AND-OR-INVERT Gate Array
DMPAL20L10	DECA 20 Input AND-OR-Invert Gate Array
DMPAL20X10	DECA 20 Input Registered AND-OR-XOR Gate Array
DMPAL20X8	OCTAL 20 Input Registered AND-OR-XOR Gate Array
DMPAL20X4	QUAD 20 Input Registered AND-OR-XOR Gate Array
DMPAL20L2	DUAL 20 Input AND-OR-INVERT Array
DMPAL20C1	SINGLE 20 Input AND-OR-INVERT Array

Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	7V	12V
Input Voltage	5.5V	12V*
Off-state Output Voltage	5.5V	12V
Storage Temperature		−65°C to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-air Temperature				0		75	°C
T_C	Operating Case Temperature	−55		125				°C

Electrical Characteristics Over Operating Conditions

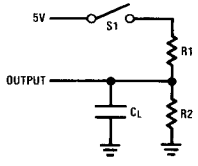
Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage						0.8	V
V_{IH}	High Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min.	I_I = −18mA				−1.5	V
I_{IL}	Low Level Input Current †	V_{CC} = Max.	V_I = 0.4V				−0.25	mA
I_{IH}	High Level Input Current †	V_{CC} = Max.	V_I = 2.4V				25	μA
I_I	Maximum Input Current	V_{CC} = Max.	V_I = 5.5V				1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min. V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL			0.5	V
			I_{OL} = 24 mA	COM				
V_{OH}	High Level Output Voltage	V_{CC} = Min. V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4			V
			I_{OH} = −3.2mA	COM				
I_{OZL}	Off-state Output Current †	V_{CC} = Max. V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.4V				−100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{OS}	Output Short-Circuit Current**	V_{CC} = Max.	V_O = 0V		−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max.	20X4, 20X8, 20X10			120	180	mA
			20L10			90	165	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX}, e.g. I_{IL} and I_{OZH}.
* Pins 1 and 13 may be raised to 22V max.
** Only one output shorted at a time.

Switching Characteristics Over Operating Conditions

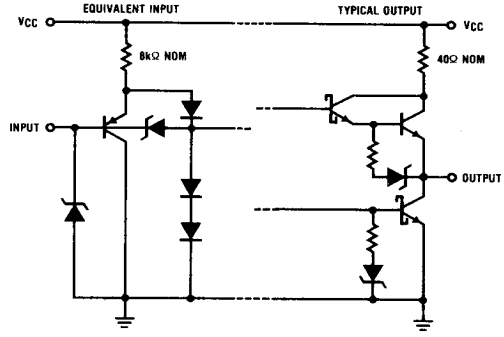
Symbol	Parameter		Test Conditions R1, R2	Military			Commercial			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	Input or Feedback to Output		20L10, 20X10 20X8, 20X4 $C_L = 50$ pF		35	60		35	50	ns
t_{PD}	Input or Feedback to Output		12L10, 14L8, 16L6 18L4, 20L2, 20C1 $C_L = 50$ pF		25	45		25	40	ns
t_{CLK}	Clock to Output or Feedback		$C_L = 50$ pF		20	40		20	30	ns
t_{PZX}	Pin 13 to Output Enable		$C_L = 50$ pF		20	45		20	35	ns
t_{PXZ}	Pin 13 to Output Disable		$C_L = 5$ pF		20	45		20	35	ns
t_{PZX}	Input to Output Enable		$C_L = 50$ pF		35	55		35	45	ns
t_{PXZ}	Input to Output Disable		$C_L = 5$ pF		35	55		35	45	ns
t_W	Width of Clock	Low		30			25			ns
		High		40			35			ns
t_{SU}	Set-Up Time from Input or Feedback			60			50			ns
t_h	Hold Time			0	– 15		0	– 15		ns
f_{MAX}	Maximum Frequency			10.0			12.5			MHz

Test Load



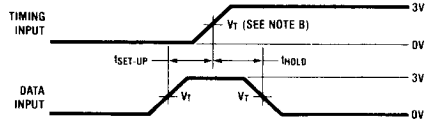
MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

Schematic of Inputs and Outputs

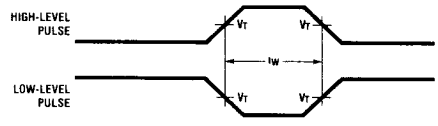


Test Waveforms

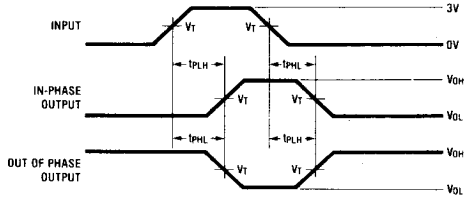
Set-Up and Hold



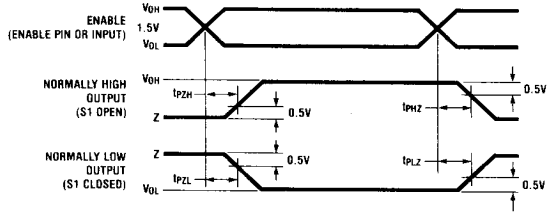
Pulse Width



Propagation Delay



Enable and Disable



Note A: C_L includes probe and jig capacitance.

Note B: $V_T = 1.5$V.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note D: All input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, $Z_{OUT} = 50\Omega$.

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all PAL types. The array is divided into two groups, products 0 thru 39 and products 40 thru 79, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}.

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9 and L/R as shown in Table 2-6.

Step 3 Select a product line by specifying A_0 and A_1 one-of-four select as shown in Table 2-7.

Step 4 Raise V_{CC} (pin 24) to V_{IHH}.

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 24) to 6.0 V.

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 24) to 4.5 V and repeat Step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 18.5 volts with V_{CC} at 6.0 volts.

Voltage Legend

L = Low Level Input Voltage, V_{IL}
H = High Level Input Voltage, V_{IH}
HH = High Level Program Voltage, V_{IHH}
Z = High Impedance (e.g. 10k Ω to 5.0V)

Table 2-6. Input Line Select

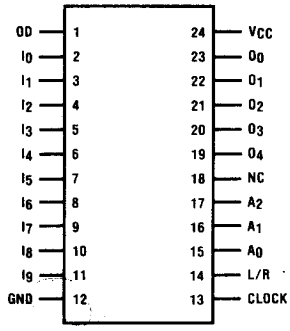
Input Line Number	Pin Identification										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Table 2-7. Product Line Select

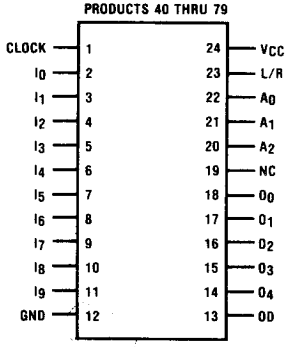
Product Line Number	Pin Identification							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Pin Configurations

PRODUCTS 0 THRU 39



PRODUCTS 40 THRU 79



Programming Parameters $T_A = 25°C$

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IHH}	Program-level Input Voltage		11.5	11.75	12.0	V
I_{IHH}	Program-level Input Current	Output Program Pulse			50	mA
		OD, L/R			50	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay Time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse Duty Cycle				25	%
V_P	Verify-Protect Input Voltage $5.5V \leq V_{CC} \leq 6.0V$		18	18.5	19	V
I_P	Verify-Protect Input Current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	ms

Programming Waveforms